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MCF5102

Addendum to
MCF5102 User Manual

December 19, 1996

This addendum to the MCF5102 User's Manual provided corrections to the original text as well as additional information not included with the manual. This document and other information on this product is maintained on the World Wide Web at http://www.motorola.com/ColdFire/.

The mask set for each part is encoded into the device topside markings. For example, the following markings would indicate a device from the 3F94E mask, manufactured in the 51st week of 1996:

XCF5102PV20A
3F94E
QEAQ9651

1. If a locked access hits in the data cache but the data cache is disabled, when the data cache is re-enabled, the next nonlocked access that misses in the data cache will not be cached. This problem can be avoided by invalidating the data cache when it has been disabled.

Masks: 3F94E 1F28T

2. To avoid the possibility of momentary bus contention of address and attribute lines, a bus arbiter must ensure that there is at least one clock after the MCF5102 BG* is negated and before the new master's BG* is asserted.

Masks: 3F94E 1F28T

3. If a locked access (TAS/CAS instruction) references a dirty entry in the data cache, it invalidates the proper cache entry and pushes this data onto the data bus. However, the MCF5102 asserts the LOCK* signal during the bus cycle for the push and keeps the signal asserted until the completion of the locked access. Therefore, to avoid this case for systems where these instructions are used for control of semaphores, locate the semaphores in cache-inhibited space.

Masks: 3F94E 1F28T

4. If a MOVE16 instruction has both source and destination addresses hitting in the same copyback mode cache line (effectively a cache line push), the source is dirty in the cache line, and the access is write protected, then the dirty cached data may be lost.

Masks: 3F94E 1F28T

5. MOVE16 (Ax) + (Ay)+ where Ax = Ay is functionally the same as MOVE16 (Ax),(Ay)+. The address register increments only once and the line is copied over itself instead of being copied into the next line.

Masks: 3F94E 1F28T

6. A bus error on a cache line push (TEA* asserted) that is initiated after the IPEND* signal is asserted to signal pending interrupt processing could cause a spurious interrupt exception instead of an access fault exception. This is a nonrecoverable bus error case that may be detected in the spurious interrupt exception handler routine and dispatched to the appropriate system error routine.

Masks: 3F94E 1F28T

7. If a write in copyback space is misaligned so that the operand request spans two cache lines, and a bus error (TEA* asserted) is asserted on the fetch of the second, third, or fourth longword of the second cache line (i.e., addresses xxx4, xxx8, or xxxC), the bus error may not be recoverable without loss of data. Specifically, if subsequent instructions also write to an address that overlaps the misaligned operand used by the original instruction, the data written by any number of these subsequent instructions can be lost. For systems that must recover from physical bus errors of this type, insert a NOP instruction after the instruction that performs the original misaligned write.

Masks: 3F94E 1F28T

8. If a line transfer is burst inhibited by asserting the TBI* signal, three additional longword bus cycles are run by the MCF5102 to complete the original line transfer. Within the tenure of these fake burst transfers, assertion of TA* during the BCLK cycles in which TS* is asserted will result in improper sequencing of the burst-inhibited line transfer. In all other cases, the MCF5102 ignores the TA* input signal when the TS* output is asserted.

Masks: 3F94E 1F28T

9. Bus snooping operation requires that accesses to shared memory space by either the MCF5102 or an alternate master must be aligned (i.e., misaligned data cache reads into a shared memory space can result in operands corrupted by intervening snoop cycles). When shared memory accesses are controlled via a software semaphore technique, the semaphore locations should not be misaligned in memory.

Masks: 3F94E 1F28T

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